Babeș-Bolyai University
Faculty of Physics
Doctoral School of Physics

Doctoral Thesis

Model calibration for simulation aided thermal design

By

Raul Cătălin CIOBAN

Scientific advisor
Prof. Univ. Dr. Simion SIMON

CLUJ-NAPOCA
2022

Contents

Keywords:

numerical modelling, reliability, thermal design, optimization, automatization

Thesis outline

The electronics industry and in particular the automotive electronics industry has seen a significant growth in the past years. Safety, comfort and functional applications have been growing and as such requiring an ever-increasing number of electronic control units. This in turn has led to the need for shorter development times and to increases in reliability challenges. To support these activities, numerical models have become a crucial tool of product development in both early stages of development when quick design decisions or changes are required but also in the later stages when reliability questions arise.

One of the main physical aspects to be considered in any ECU is the thermal management of the system. Over-heating due to high power loses, low heat exchange to ambient or simply low accuracy estimations during the definition of the cooling concept for an ECU can lead to both delays in the development process and product failures during its lifetime in the field. By creating numerical representations of a system, the thermal performance of designs can be checked and optimized for different applications. ECUs are complex systems with many connecting parts, but to have good a representation of the whole, models must be accurate down to component level. FE thermal models of electronic components with detailed internal geometry are generally not available from suppliers, or, when available, may not always meet the user's accuracy requirements for a particular application.

The current thesis is aimed at looking into both an understanding of different MOSFET packages and the particularities of the heat path through these packages and also into different methodologies for creating accurate FE thermal models based on thermal impedance measurements. The thesis is structured intro two parts and six chapters with introductory sections at the beginning of each chapter and references at the end.

The **first part** consisting of two chapters intends to introduce the reader to some general aspects of the automotive industry and theoretical concepts required for understanding the main concepts used in our studies. These aspects are followed by the initial steps taken in finding a working method for building and calibrating models. The **second part** is divided into three chapters that describe the calibration process of different MOSFET packages using different methodologies. Each chapter present a new development in our modelling process building on the experience gained in the previous step.

The **first chapter** entitled "*Introduction to electronic assemblies and theoretical concepts of thermal assessment*" starts with a short history and overview of the growing trends in the automotive industry to help the reader understand the necessity of new technologies in product development. It continues with a description of electronic assemblies and their thermal reliability. Further in the chapter the basic theoretical concepts of heat transfer principles and thermal metrics such as the thermal resistance and thermal impedance are discussed in detail. The chapter ends with theoretical concepts of finite element method (FEM) and its implementation of the thermal domain in simulations.

The **second chapter** entitled **"*Methodology and model preparation*"** describes the devices measured and calibrated in out studies together with the methods used to achieve this. The first method discussed refers to a description of the thermal impedance measurements (Z_{th}). The following methods present the analytical measurements used in determining the inner structure of the DUTs and the steps used in creating a CAD geometry. Using these inputs, the

next part focuses on simulation model setup and relevant sensitivity studies of its parameters. For the final section of this chapter, the two model calibration concepts used in the following chapters are briefly discussed.

The **third chapter, "*Model calibration of MOSFET package using T3ster measurements and structure functions*"**, is focused on the buildup and understanding of an LFPak88 discrete package. The work aims to measure all three heat paths and calibrate the simulation model for an accurate representation of all three. This is done through Z_{th} measurements and structure function (SF) transformations. Using test boards on which the device is soldered and the equivalent simulation representation of the setups, the calibrated model is validated.

In the **fourth chapter** "*Towards automated model calibration*", a new method for calibrating components is discussed. Using a D2Pak (TO-263) package from Infineon as the device under test (DUT), T3ster measurements are carried out for a slug-down configuration. Initially the model is successfully calibrated through the same method as the one in chapter three. After the successful calibration using the iterative method, a new method is presented based on commercially available optimization algorithms. The study ends with a comparison of the two and argues for the advantages of direct calibration of Z_{th} curves in an automated manner versus the manual process using structure function transformations.

The **fifth chapter** "*Complete heat path calibration of power MOSFETS via automated optimization*" builds upon the experience gained during the studies discussed in the previous chapters. The automated method argued for in chapter 4, is further used on two different components in LFPak56 and LFPak56D package. While in chapter 3 we have used the manual method to calibrate all heat paths through an LKPak88 package and in chapter 4 we have focused in finding a workflow for a direct and automate Z_{th} calibration, in this chapter the two come together. An update to the methodology is made to simultaneously adjust all properties for each hat path using optimization algorithms.

The **final chapter** gives an overview of the conclusions and the main contributions of the paper.

While the derived properties for each package are particular to its corresponding model, the differences found from literature values, highlight the importance of calibrating models based on measurements. The outlined methodology in this final chapter can be successfully applied to measuring and modeling any particular MOSFET package resulting in high accuracy, readily available models for thermal design.

Chapter 1

Introduction to electronic assemblies and theoretical concepts of thermal assessment
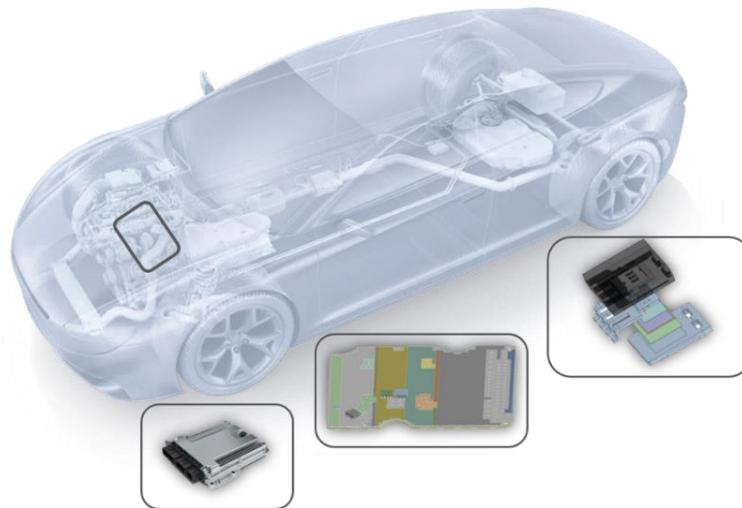
1.1 Automotive electronics

In the automotive industry, the first electronic control unit (ECU) was used for the purpose of electronic injection. In 1953, before the development of the first Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs) and microcontrollers, the Bendix Corporation started developing the first commercial EFI "*Electrojector*" [1,2] Based in part on this technology, Bosch developed its first electronic fuel injection system called "*Jetronic*" in 1967. A more widespread use of electronics in the field came in the beginning of the 1970s when the development of MOS integrated circuits and microprocessors has led to a new range of applications in the automotive industry such as airbag control units, transmission control units (TCU), adaptive cruise control (ACC), electronic stability program (ESP) and others. [3]

These have led to a growth of the automotive electronics industry during the last decade with ever-new applications (Figure 1a)coming to answer customer needs. Quantitatively, this can be seen in the contribution of the total cost of electronics to the cost of a vehicle (Figure 1b), which increased from roughly 5% in the 1970's to 35% in 2010 and forecast to increase up to 50% by 2030 [4]. The number of electronic devices and components built into cars these days are on the rise, and the reliability of the electronic components used in the controlling devices is having a growing impact on the reliability of the vehicle overall.
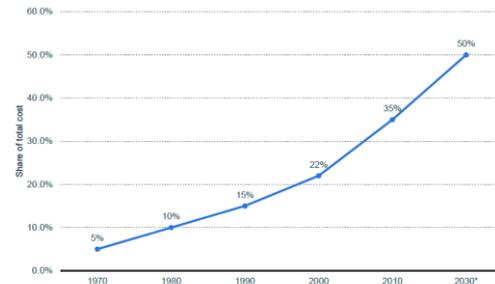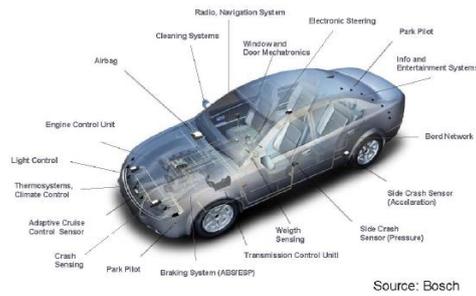
Figure 1. *(a) Current usage of electronic control units (ECUs) in commercial vehicles [1];(b) Automotive electronics cost as a percentage of total car cost [4];*

1.2 Electronic assemblies and thermal reliability

Reliability of ECUs is an integral part of their design process. All design elements of the assembly from the basic circuit elements such as transistors, resistors and capacitors to the printed circuit board and enclosure of the electronics have to be considered and chosen based on the required application.

Modern electronic assemblies are based primarily on a series of metal-oxide-semiconductor (MOS) transistors and integrated circuits mounted on printed circuit boards (PCBs). Together with the passive elements of the circuit such as resistors and capacitors, they make up the printed circuit board assembly (PCBA) which can now accomplish the electronic function it was designed for. The PCBA (Figure 2) is generally connected to other mechanical parts such as connectors or housings with each having a specific role in the design of the ECU.

Figure 2. *Example of a PCB assembly with components [5]*

Electronic failures can result from a variety of factors such as design, component and manufacturing processes, overstress, and maintenance. Depending on the time of failure, they can be classified into three distinct classes: early-life, event-related and wear out [6].

Most failure assessments and life-time predictions can be done through testing, which is possible only in the final stages of product design when it often becomes difficult and expensive to implement changes.

1.3 Thermal theory

Heat transfer is based on three modes of transport: through **conduction**, **convection**, and **radiation** processes. Each process is based on a different transport law. [7]

In practice we will generally require the one-dimensional heat ***conduction*** equation (Eq. 1).

$$\frac{\partial^2 T}{\partial x^2} = \frac{\rho c}{k} \frac{\partial T}{\partial t} = \frac{1}{\alpha} \frac{\partial T}{\partial t} \tag{1}$$

The second mode of transport for heat is ***convection*** which is the process of heat removal from a sold body by a moving fluid. This is represented by Newton's law of cooling in its steady state form:

$$q = \bar{h}(T_{body} - T_\infty) \tag{2}$$

where $\bar{h}$ is the average heat transfer coefficient over the entire surface of the body, h would be the local value at a given position.

The third and final mode of transport is through thermal ***radiation***. The amount of energy emitted by a body depends on its temperature and surface properties. Since the emission varies as the fourth power of absolute temperature cooler bodies will emit less energy than hot ones. Experimentally, the radiation law was determined by Stefan in 1879 and explained by Boltzmann based on thermodynamics in 1884 that for a black body the relation between e(T) and T is:

$$e_b(T) = \sigma T^4 \tag{3}$$

where σ is the Stefan-Boltzmann constant and its value is 5.670374 x 10^{-8} W/m^2*K^4 and T is the absolute temperature. [7]

The **thermal resistance *(R$_{th}$)*** is generally defined as the ratio of difference between the temperature Ta and Tb of two given points, and the conductive heat flux ϕ_q flowing between them.

$$\theta_{ab} = \frac{T_b - T_a}{\phi_q} \tag{4}$$

In thermal characterization of a system, it is also important to consider the amounts of energy stored by each material though it's heat capacity. This is done through the **thermal impedance** *(Z$_{th}$)* **of the system.** Using the electrical analogy (Figure 3) discussed above, these can be modeled as capacitors.

Figure 3. *Representative view of a one-dimensional heat path*

The definition of the concepts and the standards for measuring the R_{th} and Z_{th} of a semiconductor device with a heat flow through a single path is found in the JEDEC JESD 51-14 standard [8].

To understand the contribution of each element in the heat path to the total thermal impedance response is not trivial as it is a sum of thermal resistance and capacitances. In this regard a series of mathematical transformations are used to convert Z_{th} curves into a continuous lumped capacitance and resistance called a structure function (Figure 4) [9].
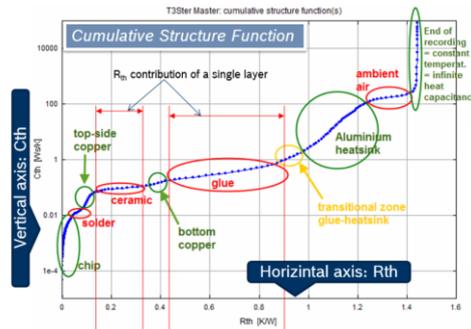
Figure 4. *Example of interpreting a structure function [10]*

1.4 Finite Element Method

To describe the behavior of multi-component systems, it is common practice to divide it into individual components or what we may call "elements" which have a well-known behavior. Based on the understanding of each element, the more complex system can be then rebuilt. What we call a "discrete" problem is described by a finite number of such well-defined elements. If the division into elements would continue indefinitely, the problem would become "continuous" which is closer to the true nature of physics and engineering problems.

The finite element process as defined by O.C. Zienkiewicz et. all is a method of approximation to continuum problems such that:

(a) the continuum is divided into a finite number of elements, the behavior of which is specified by a finite number of parameters, and

(b) the solution of the complete system as an assembly of its elements follows precisely the same rules as those applicable to standard discrete problems. [11]

There is a significant amount of software applications that solve these types of discrete systems. In our studies we have used the Ansys Mechanical solver which implements the thermal field differential equation in its matrix form as:

$$[C]\{\dot{T}\} + [K]\{T\} = \{Q\} \tag{5}$$

where [C] is the capacitance matrix, [K] is the conductivity matrix and Q is the heat flow.

1.5 Conclusion

In this chapter, the main theoretical concepts related to thermal theory and computer aided design have been introduced and discussed. These points are essential for our goal in understanding and developing the methodology for detailed modeling of the basic elements in a thermal system. To complete the picture, in the proceeding chapters, additional theoretical content together with the state-of-the-art use cases will be introduced.

The model calibration procedure is relatively straight-forward:

i)   Record a thermal measurement of the device under test

ii)   Build up a virtual representation of the said device

iii)   Set up the initial simulation model

iv)   Adjust the model parameters to fit the measured response

Throughout the thesis we present our process starting from this fundamental procedure, continuing with the in-depth study of each step, and refining our approach to reach an optimal procedure which gives reliable and accurate results.

Chapter 2

Methodology and model preparation
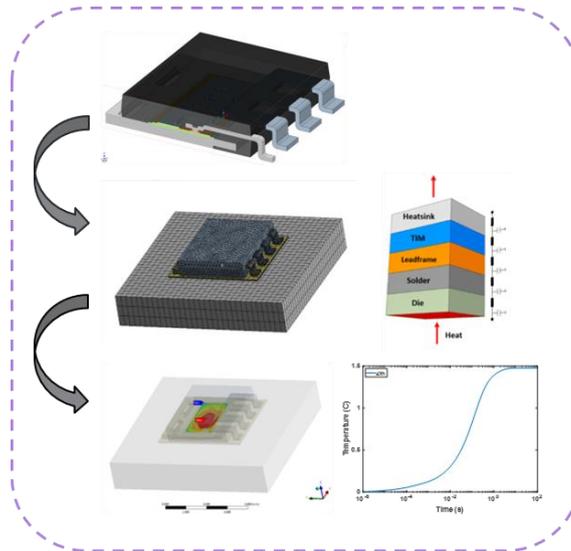
2.1 Introduction

The current chapter comprises of all the necessary steps taken in the initial phase of our studies. Everything from the methodology in handling the thermal measurements to the analytical methods used in describing the geometry of the devices and the numerical model, is included.

2.2 Devices under test

Due to both the importance and number of MOSFETs in electronic design, these types of components were chosen as the pilot device for the current study. Four packages were studied (Figure 1).
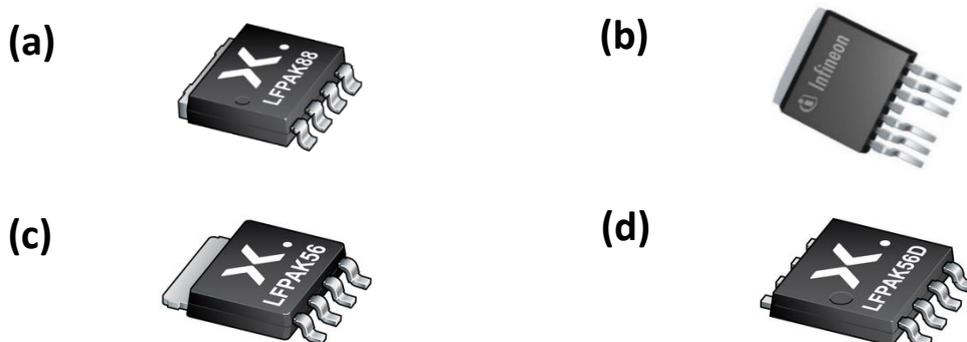
Figure 1. *a) BUK7S1R0-40H (LFPak88) [12]; b) IPB180N06S4-H1 (D2Pak) [13]; c) BUK7Y1R7-40H (LFPak56) [12]; d) BUK7K6R8-40E (LFPak56D) [12]*

2.3 Measurement methodology

In our work, we used temperature sensitive parameter (TSP) measurements. The TSP measurement is common for measuring the thermal behavior of semiconductors and it can be described by a variety of parameters such as a diode voltage drop, a gate to source voltage drops, an emitter current, etc. We have used the diode forward voltage as it is, according to the JEDEC standard, the most common used technique. To measure the thermal impedance curve, a negative power step is required. We have used the T3ster measurement equipment developed by Mentor Graphics.

Three setups were used in our initial measurements to isolate each of the three heat paths in a MOSFET device. The slug-down configuration is done by fixing the DUT on a strip of thermal interface material (TIM) which is further fixed to a water cooled heatsink. A similar configuration is used for the slug-up measurements. For the pin cooling setup, the pins of the DUT are soldered to a large copper block which is then fixed though a TIM layer to the heatsink.

2.4 Preparing the CAD

A detailed inner structure of the package is required for an accurate representation of the heat path through the component. In this regard, there are several analytical techniques available such as **cross-sectioning**, **computer tomography** (CT) and **chemical de-capsulation**. All three methods were used in our study to gain a good understanding of the investigated packages.

Using the analytical techniques mentioned above, reference pictures and measurements for the model have been generated. The data was then further used in the commercially available **CAD** software **Ansys SpaceClaim** to create both the component model geometry and also a simplified geometry for the measurement setup (Figure 2).
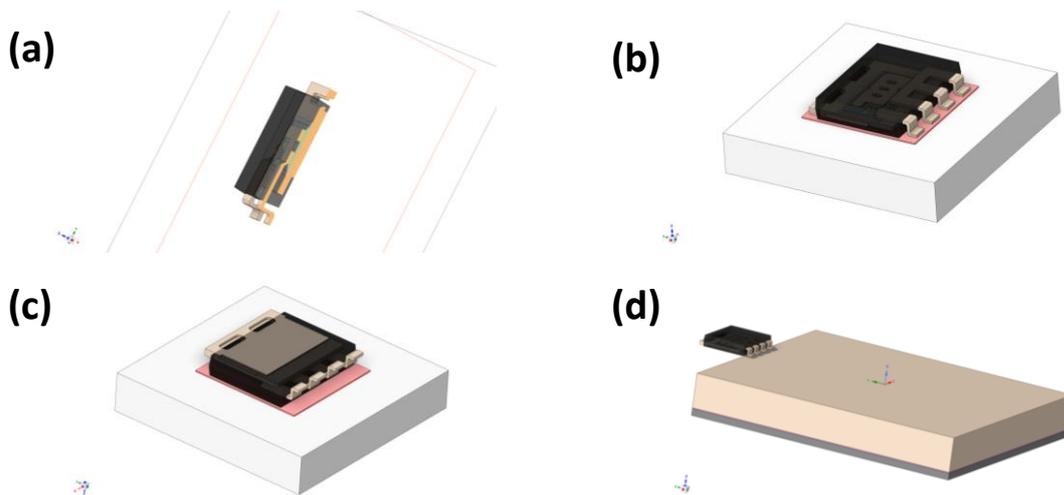
Figure 2. *(a) Geometry generation based on measurements; (b) DUT with slug down setup; (c) DUT with topside cooling setup; (d) DUT with pin cooling setup*

2.5 Initial model setup

Once the geometry has been generated, we must now define the mechanical model settings. As we have discussed in chapter 1, the first step in the process is the discretization of the model (Figure 3).
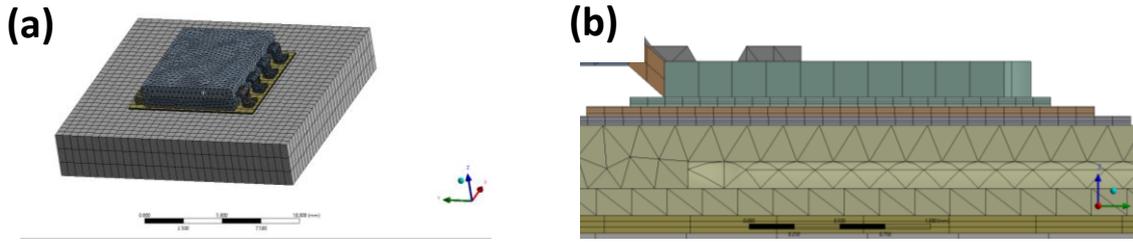
Figure 3. *(a) Overview of mesh for component together with slug down setup; (b) Detailed view of component inner structure mesh*

The first parameter of the thermal analysis is the initial temperature of the system. As both the R_{th} and the Z_{th} are based on the temperature increase and not on absolute temperature, it is convenient to set it to 0^0C. For the initial approach of our study, for the LFPak88 and D2Pak, we have used a surface heat flux defined to 1W. As we are representing a 1D heat flow for simplicity a temperature boundary condition of 0^0C was set on the heatsink. In figure 4 we can see the implementation of these parameters.
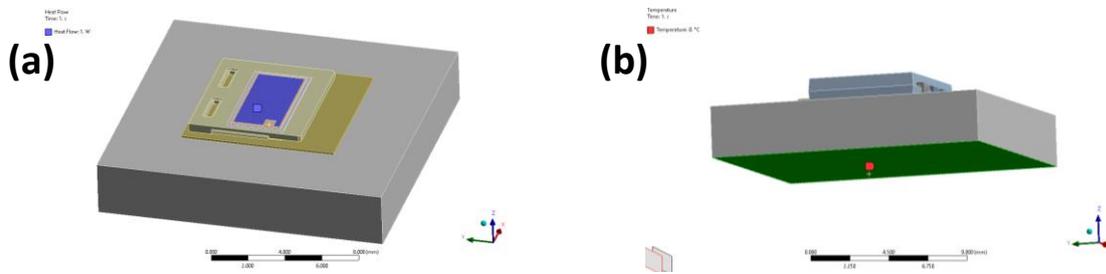
Figure 4. *(a) 1W heat flow applied to the surface of the active region of the chip; (b) temperature boundary condition applied on the bottom of the setup*

The final step is evaluating the results. For our purposes we are evaluating the average temperature of the same region used for applying the power load (Figure 5).
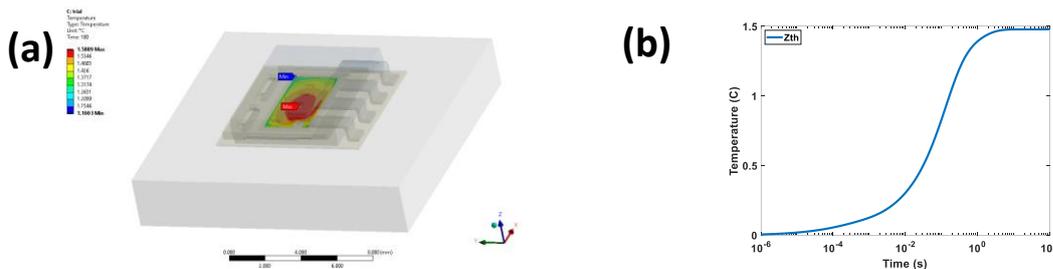
Figure 5. *(a) Temperature evaluation of chip surface; (b) Z_{th} plot of the system*

2.6 Sensitivity studies

In reaching the process outlined above, sensitivity studies were carried out at the beginning of the workflow to understand what the best values are to use for parameters such as **mesh** and **time stepping** and what is the impact of **convection** when assuming the 1D heat flow to the heatsink.

12

2.7 Model calibration

2.7.1 Manual calibration

The simulation is run with initial material properties based on literature and the average temperature of the die is extracted. The transient representation of this rise in temperature with respect to the power dissipation is defined as the $Z_{th}(t)$ [14], which describes the entire heat path through the component. While comparing these Z_{th} curves provides a good starting point, just by using a direct comparison it is difficult to identify which layer inside the component requires adjusting. As such, the structure function is used as a representation of the cumulated resistance (R_{th}) and capacitance (C_{th}) of the entire heat path based on Cauer - Foster (Figure 6a) transformations. A schematic view of this simplification of the heat path is shown below (Figure 6b).
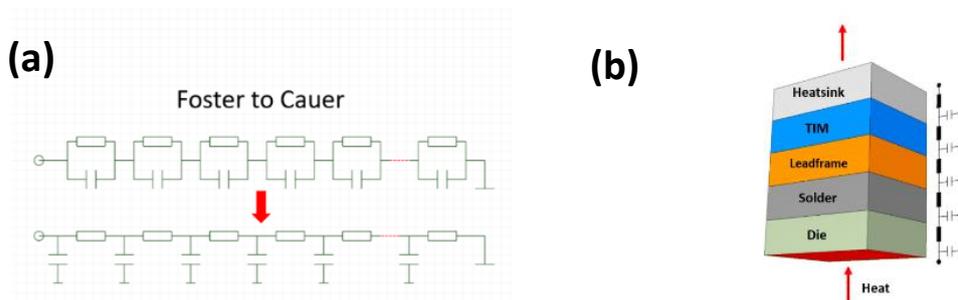
Figure 6. *a) Foster – Cauer conversion; b) Schematic of heat path*

The transient behavior of a body is influenced by three main material properties: thermal conductivity, density and specific heat. The adjustment of the SF is done by changing the material property for each layer inside the component starting from the silicon chip. The schematic of this approach is shown below in Figure 7.
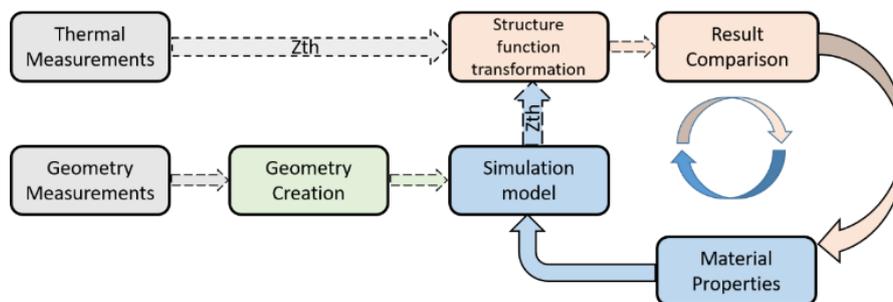
Figure 7. *Iterative calibration schematic*

2.7.2 Automated calibration

The second method is based on an automated calibration using optimization algorithms. Unlike the previous method that requires mathematical approximations for structure function derivation, this method allows for the direct fitting of Z_{th} curves. Using the same general considerations and boundary conditions as in the previous method, a material property sensitivity study is defined in Ansys using the optiSlang plug-in and the DoE method.

Based on the output of the design points, a Metamodel of Optimal Prognosis (MOP) is generated. The MOP is based on the search of the optimal input variable set and the most appropriate approximation model [15]. The number of available design points and the range in

which these were derived directly affects the accuracy of the MOP. Starting from these results, the optimization is done with a series of algorithms.

The first algorithm used in the optimization stage is the Evolutionary Algorithm (EA). After obtaining the optimal design from the evolutionary algorithm, the resulting parameter values are passed on to a Nonlinear Programming by Quadratic Lagrangian (NLPQL) algorithm [16].

The measurement results (Z_{th}) are used as a reference in the optimizers. By minimizing the error between the measurement and the predicted simulation results at discrete time points, the corresponding material properties for the calibrated design are identified.

2.8 Conclusion

In this chapter we covered a series of crucial points relevant to the following work such as: description of the measured devices, the measurement equipment and setup, the analytical measurements required for CAD generation and a short overview of model setup and calibration approach. All the necessary analytical and numerical methods have been investigated and can be readily transferred to set up the methodology for model calibration which is the final target of this thesis. In the following chapters the methods will be applied to four specific packages under study.

Chapter 3

Model calibration of MOSFET package using T3ster measurements and structure functions
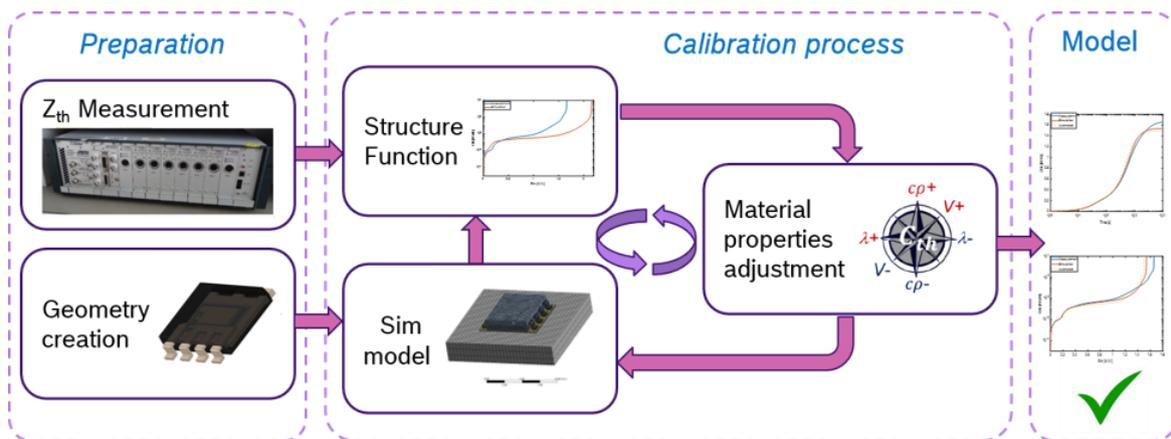
3.1 Introduction

The scope of this paper is mainly to present the challenges of thin package MOSFETs' measurements and FE model calibration using structure functions [9]. Second, it is to validate the calibrated model using test boards, and to show the usefulness in studying the impact of different footprints and PCB layout details on overall cooling performance. Components in LFPAK-style package were chosen as test specimens for the current study due to ever-stronger miniaturization trends.

3.2 Experimental and numerical methodology

In our presented approach, we chose the following three conductively cooled test setups for a complete thermal characterization of the studied power MOSFET package [17]:

1. "slug-down" or bottom cooling (drain tab on water-cooled cold plate, pins in the air)
2. "through-pin" cooling (pins soldered to a copper block, which in turn is attached to a cold plate, drain and package body in the air)
3. "through-mold" or topside cooling (plastic mold on cold plate facing down, drain tab facing up towards air)

Thermal impedance measurements have been carried out using commercial T3Ster™ equipment.

The optimization process used for calibration is a manual, iterative approach. This method is used to successively calibrate all three heat paths of the component, first starting with the main path though the slug.

For the FE model simulation, two commercial software packages were used: an FEA solver Ansys Mechanical and a CFD solver Mentor Graphics FloEFD. This approach was chosen in order to establish if the derived models are valid and interchangeable between different software packages with different solvers.

3.3 Results and discussions

The component chosen for characterization is a BUK7S1R0-40H type power MOSFET in LFPAK88 (SOT1235) package, made by Nexperia. This component was chosen as the current study object due to its novel package design concept, high thermal performance, and the foreseeable importance of auxiliary heat paths when mounted on PCB. The main structures in the heat paths of the LFPAK88 package are the silicon die, solder die attach on both sides of the silicon chip, copper slug at the bottom and copper clip at the top.

3.3.1 Thermal impedance measurements

The slug-down test setup and measurement results are shown in Figure 1. The water-cooled heatsink provides a low-resistance heat path to the 25 °C water. $R_{th\_junction-to-water}$ was measured in the range of 1.7 K/W, and the R_{th_JC} of the DUT was found to be around 0.3 K/W (TDIM method, [8]).
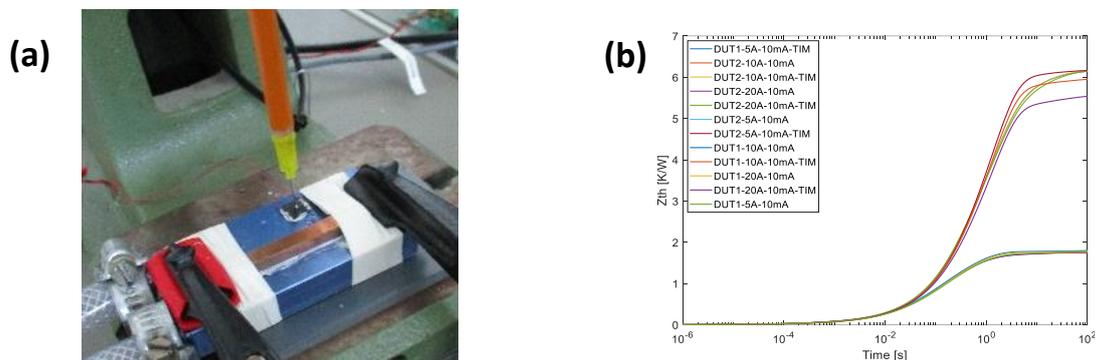
Figure 1. (a) *Slug-down cooling test setup, with one of the water-cooled cold plates used in the experiments. (b) Sample Z_{th} results of slug-down cooling setup, with and without TIM, using different heating currents. Upper curves are without TIM, lower curves with TIM.*

The through-mold cooling test setup (Figure 2) is very similar to the previous one, but the DUT is placed with the mold compound facing down, toward the heatsink, with addition of a TIM layer, while the metallic Drain tab is facing up, into the air. Rth_junction-to-water was measured in the range of 15-20 K/W, and the Rth_J-Top of the DUT was found to be around 4 K/W, using TDIM method [8].
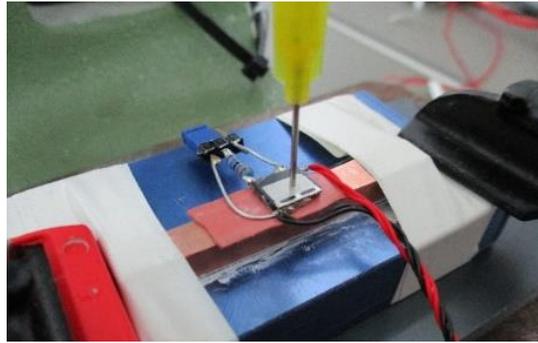
Figure 2. *Details of the through-mold cooling test setup.*

For through-pin cooling tests, the setup consisted of five DUTs soldered to a flat copper block (~100 x 50 x 5 mm), as shown in Figure 3a. The copper block was attached to a water-cooled cold plate using TIM. Measurement results are shown in Figure 3b.
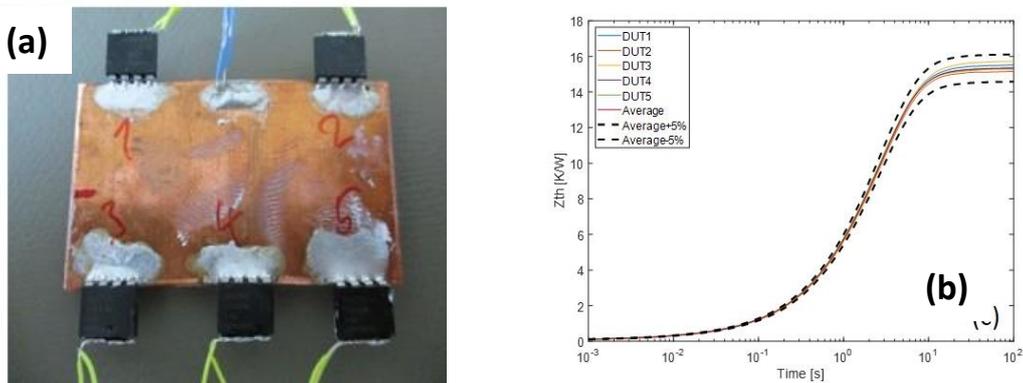
Figure 3. *(b) Pin cooling measurement setup; (c) Measured Z_{th} curves of pin-cooling test setup (n=5, p=5%).*

3.3.2 Geometry creation

Based on cross-sections, chemical decapsulation and X-Ray imaging, a geometrical model was adjusted using a CAD software SpaceClaim (Figure 4a, b).

To have an accurate representation of the power load surface area, a separation between the active and passive areas was done. This was done based on coverage area of the top solder (clip solder).

For representing the measurement setups of the three configurations, estimations were made for the TIM dimensions and heatsink.
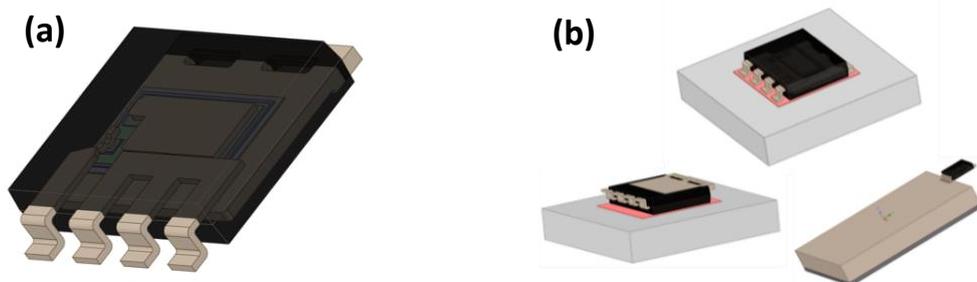
Figure 4. *(a) geometry; (b) setup overview*

17

3.3.3 Optimization

For calibration of the main heat path, the slug-down cooling setup was used. Assuming a simplified 1D-heat flow, this would reduce the problem to identifying and fitting three layers in the structure functions: silicon die, solder, and bottom copper. By analysing the structure functions corresponding to the measurement Z_{th}, three distinct regions of the slug down heat path inside the component can be identified. The first region up to 0.05 K/W may be assigned to the heat flowing through the die. The second characteristic between 0.05 and 0.09 K/W representing the heat flow though the solder beneath the silicon. The third and final distinguishable characteristic is between 0.09 and 0.3 K/W and it describes the heat flow through the thin copper slug. The thermal resistance beyond 0.3 K/W corresponds to heat passing through the thermal interface material and cold plate heatsink.

The calibration of the model (Fig 5a, b) was done by a similar analysis of the structure functions calculated from the simulated Z_{th} responses, in which the corresponding R_{th} and C_{th} of each layer was identified and compared to the measurement results. Based on these findings, subsequent adjustments of the thermal conductivity (TC) and density of each structure in the heat path were done starting from the silicon die and moving outwards to the heatsink. After each material property change, a new simulation was run, and a new comparison was made.

The next step in the modelling process is calibrating the material properties of the secondary heat paths through the pins and the mold (Fig 5c, d). The measurement setup of the pin cooling was the first setup built with similar boundary conditions to the slug down cooling. Using the same assumption of a 1D heat path would reduce the problem to identifying and calibrating the material properties of the clip solder and copper clip.

The final step in the component calibration process involved the comparison to the top-side cooling setup measurement. Using the same setup as for the slug down cooling, the component – now with updated material properties – was rotated and positioned with the mold in contact with the TIM. Due to the pin cooling calibration having a representation of the mold as well, no additional calibration was necessary, and the model rather confirmed the calibration results from the previous steps (Figure 5e, f).

The resulting properties (Table 1) are different from the generally expected values for the corresponding materials. Although the smaller differences in the copper slug properties can be attributed to geometrical tolerances, the conductivity of the silicon and solder have obvious deviations from what one may consider physically plausible values, and it's difficult to attribute just to geometrical influences.
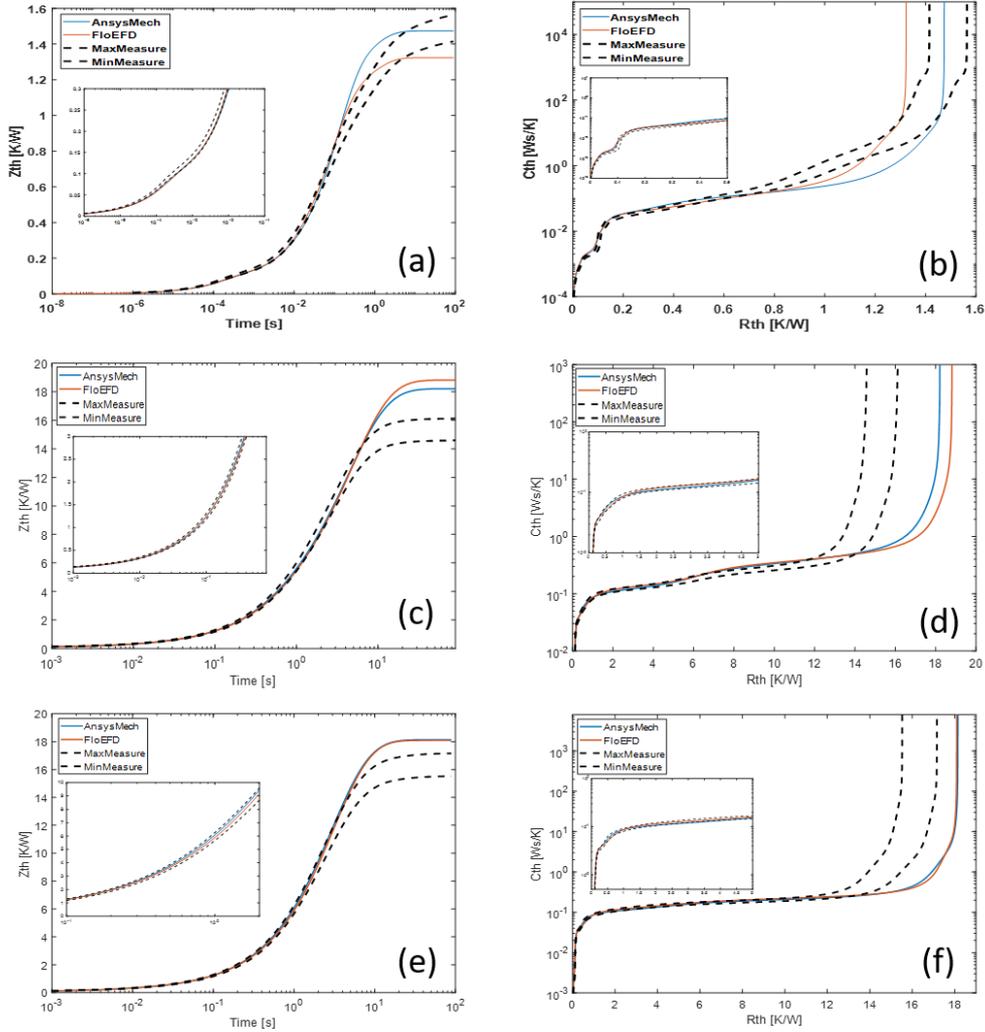
Figure 5. *(a) SF of the slug down calibration (b) Z_{th} of the slug down calibration (c) SF of the pin cooling calibration (d) Z_{th} of the pin cooling calibration (e) SF of the top side cooling calibration (f) Z_{th} of the top side calibration*

Table 1 Calibrated material properties for a transient correction of 40-180 μs

Material/Prop	Density (Kg/m^3)	TC (W/mK)	Specific heat(J/KgK)
Silicon	2300	40	1000
Solder chip	8400	100	210
Solder clip	3200	20	210
Copper slug	10000	450	280
Copper clip	8300	310	280
Mold	4000	1	820

3.4 Model validation

Our test vehicle followed this reasoning: if there is no way to get precise verification of the package model in PCB based experiments, at least we should be able to prove that by further simplification of the model (e.g. disabling one of the secondary heat paths) the response would be way off. This task is possible to implement in a layout that cools both the Drain tab and the Source pins in an equal way. Such a layout is shown in Figure 6.

19
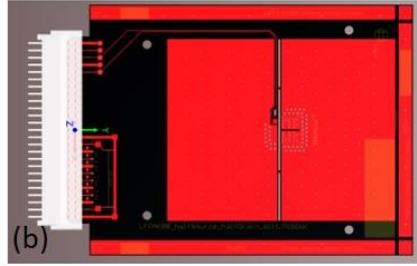
Figure 6. *Test card used for model validation, top layer copper of the layout.*

This two-sided PCB features large, dedicated cooling areas for the copper slug (drain) and source pins of the component. In the PCB layout, the FR4 between the two areas was also removed (with "slits") to lower the thermal interaction, and physically separate the two areas. This way the setup can exercise the two most significant heat paths of the component (through the slug and through the pins) and the setup simulations are expected to show significant differences between the calibrated and non-calibrated models.
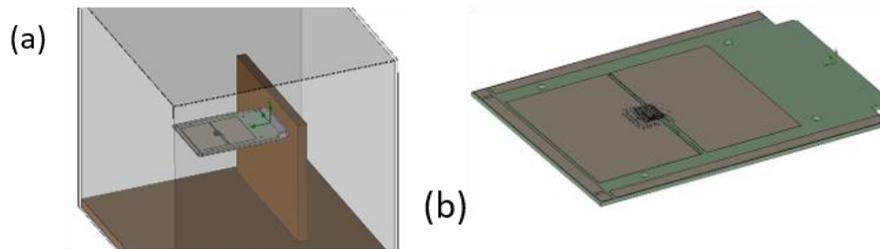
Figure 7. *(a) CAD model of the test PCB in the JEDEC still air chamber (used for airflow simulation); (b) Detailed FE model of the test PCB with the mounted LFPAK88 component (including explicit vias in the footprint)*

Both measurement and simulated data evaluation showed that R_{th-JA} values of the PCB test setups placed in still-air chamber are very large (>15 K/W) compared to the R_{th-JC} value of the components (<0,5 K/W). This means that the overall thermal performance is dominated by the heat spreading in the PCB, and the PCB-to-air bottleneck, and the measurement features poor signal-to-noise ratio in the early time range (<100 ms) of the Z_{th} because of the limited allowable power dissipation, and small temperature swings within the LFPAK88 package. However, if we manually "detune" our component model (by changing material parameters or changing the geometry), the relative contribution of the two main heat paths within the component will also change, and the different utilization of the large drain and source copper areas of the PCB will show a visible effect on the simulated results. This can be clearly seen on the thermal impedance and structure function responses of the different simulation models (Fig 8a, b). The component model with the correct geometry and materials fits the measurement within 5% tolerance range, while the component model with the same geometry but not calibrated (standard library) materials show a too optimistic result, in this particular case.

Also, if we simplify the LFPAK88 component model by removing elements of the copper clip, as if no information would be available about the internal structure, (Fig 8a, b) result, showing significant mismatch not only in the early component transient, but also in the later parts. Steady-state values become higher by >20%, which is a good proof that modelling

the heat transfer through the pins is a necessity for a universally applicable LFPAK88 thermal model.
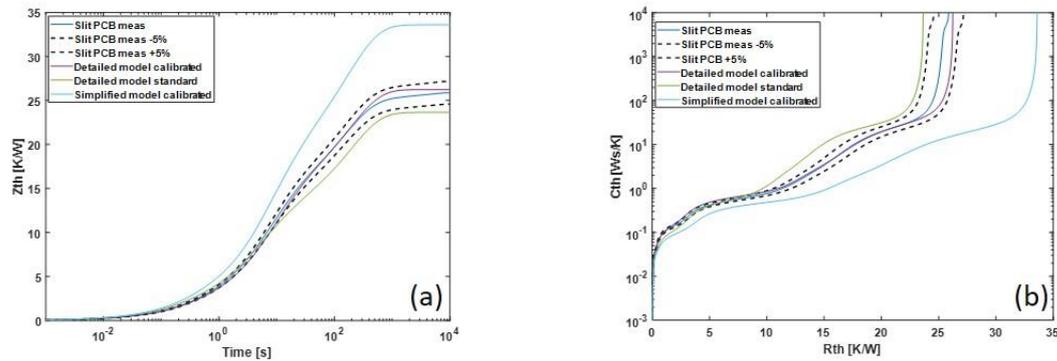
Figure 8. *(a) Comparison of the measured and different simulated thermal impedance curves; (b) Comparison of the measured and different simulated structure function curves.*

3.5 Conclusions

The component was measured, and its model was calibrated using the comparison of the structure function based on an iterative approach, adjusting the different material properties of the layers. The resulting model exhibits an extremely good match to the measured reference datasets.

The tuned model was checked against an independent measurement for validation, using a PCB test board. FE simulations showed a reasonable match with measured data and showed that the revised PCB test card design (where equal copper cooling areas are allocated to both Drain and Source) is a suitable test vehicle to prove that no further simplifications are possible, and therefore all existing details are required in our tuned model.

Obtaining a reliable simulation model with very good agreement to measurement opens the way to assess and compare thermal performance of different footprint variants. This information is relevant when developing new products and ensures that the optimal design is reached in terms of thermal performance and manufacturability.

Chapter 4

Towards automated model calibration
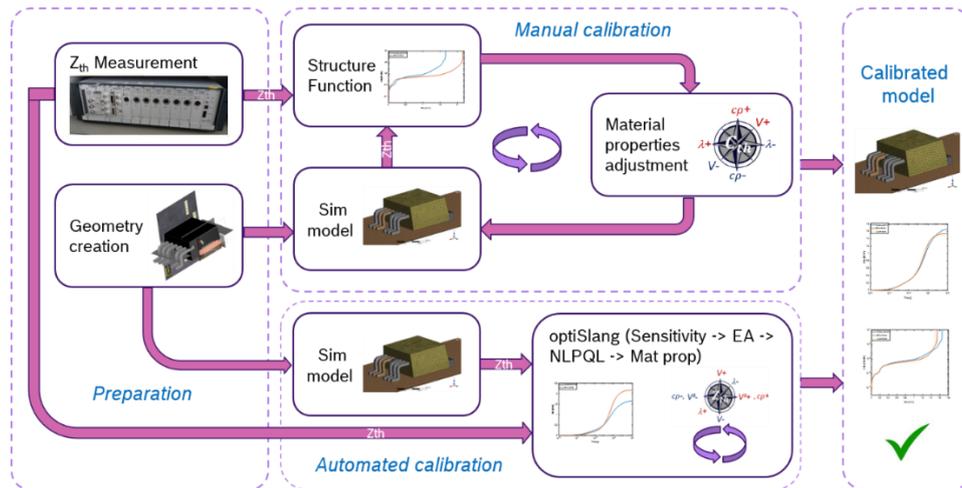
Reproduced from: FEM model calibration for simulation aided thermal design, Microelectronics Reliability, Volume 118, 2021, 114042, ISSN 0026-2714, doi: 10.1016/j.microrel.2021.114042.

4.1 Introduction

In the current chapter, the aim is to define and create an accurate simulation model, which has a low error in both transient and steady-state simulations. The methodology by which reliable numerical models can be derived for electronic components starting from thermal measurements is described herein. During the model tuning process, the sensitivity of each layer of the component can be investigated and their impact on the thermal behavior can be determined identifying the critical parameters for the thermal representation of the component. Further, based on the considerations derived from the iterative calibration, an automated method using OptiSlang is used, and the resulting model is verified by comparison to the iterative calibration highlighting the advantages it brings.

4.2 Theoretical considerations

The fundamental theoretical considerations used in describing thermal behavior of electronics are the thermal resistance and thermal impedance metrics discussed above.

In the development activities of the automotive industry where the component is just a part of the larger system, it is desired to have accurate, reliable models in a short amount of time. The logical approach would be to steer towards automation methods, which eliminate the

drawbacks of user-handled iterative approaches detailed in the previous chapter. Moving further, an alternative approach for component modelling was studied using a commercially available optimization software, namely OptiSLang.

4.3 Methodology and equipment

4.3.1 Measurements

Reference data for the model tuning process was obtained by measuring thermal impedances (Z_{th}, step response) of the studied devices, while the device under test (DUT) was placed in an adequate test setup (similar to the previous test case).

Measurement data was gathered from several DUTs of the same type, and experiments repeated, to check both sample-to-sample and our test setups' variability (Figure 1).
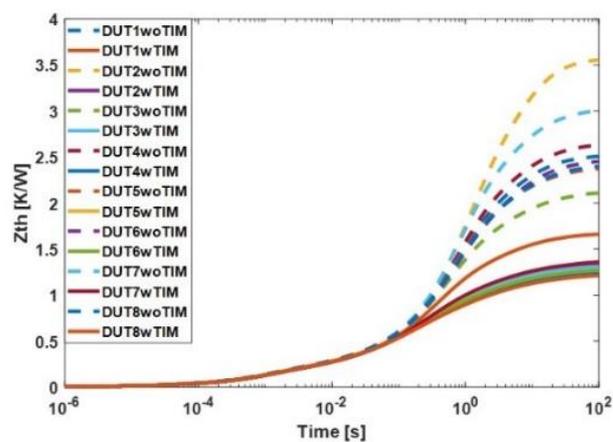
Figure 1. *Measurement results with and without TIM*

4.3.2 Geometry creation

The component used for demonstrating the concepts of this paper is an IPB180N06S4-H1 device in D2Pak (TO-263) package from Infineon. The geometry (Fig. 2) was constructed based on the official data sheets, cross-sections, and Computer Tomography (CT) scans. The size of the package was determined using the data sheet together with optical microscope images.
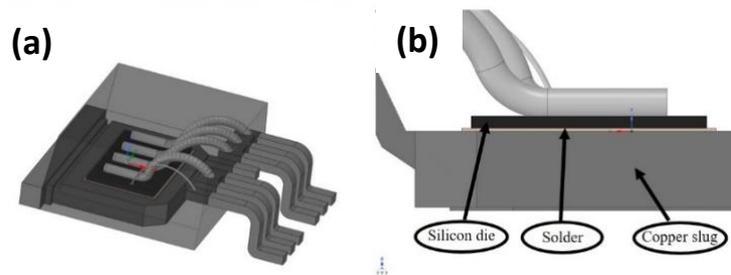
Figure 2. *(a) Overview of component geometry; (b) Component inner structure.*

4.3.3 Pre-requisites of the simulation model

The simulation model was created using a commercial FEA software (ANSYS). The initial material properties (Table1) were set up considering "realistic" values (based on literature and previous experience) for each material type: silicon for die, solder for die attach, aluminum for bonding wire, plastic for the mold material and copper for the pins and the slug.

23

Table 1 Estimated material properties

Component (Material)	Density (Kg/m^3)	Thermal conductivity (W/mC)	Specific heat (J/kgC)
Die (Silicon)	2300	80	1000
Die attach (Solder)	8400	55	210
Slug/Pins (Copper)	8300	310	280
Mold (Plastic)	2000	0.7	820
Wire bonds (Aluminum)	2689	237.5	951

Considering the definition of the thermal resistance $R_{th}=(T_j-T_{amb})/P$ and the fact that temperature dependent material properties are not used, the ambient temperature was chosen as 0^0C and the 1W power dissipation was applied as a Heat flux on the surface of the die. The same 0^0C is used as a temperature boundary condition on the bottom of the test setup to represent the cooling via the heatsink (Figure 3). For evaluating the thermal response, the average temperature of the top surface of the die was used.
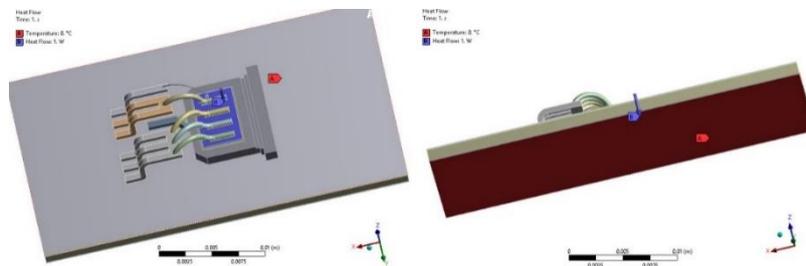
Figure 3. *Simulation model*

4.4 Component calibration

4.4.1 Calibration using structure functions and an iterative approach

The simulation model was run with the assumptions presented above and the Z_{th} curve was compared to the measurement. Comparing the two Z_{th} curves, a significant difference can be seen in the microsecond to millisecond time frame where the behavior of the component is described. Beyond the first 0.1 seconds, the Z_{th} is predominantly influenced by the configuration of the setup (TIM and heatsink). By the sheer comparison of the two Z_{th} curves (Figure 4a), it is quite difficult to identify which material parameter within its specific layer stack requires adjusting. As such, a different approach should be employed for the fitting process. From the two available measurements, with and without TIM, the R_{th} of the component was determined to be 0.34 K/W by using TDIM method.
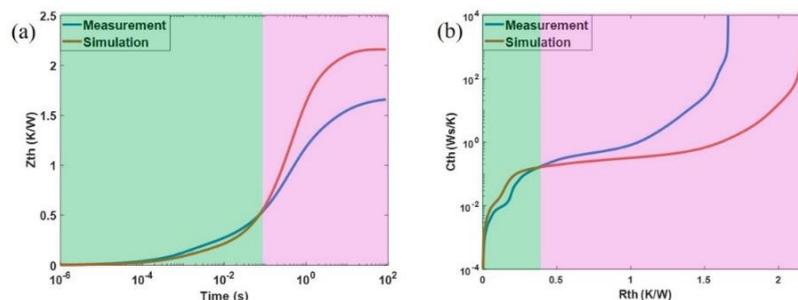
Figure 5. *(a) Z_{th} curves of the measuremnt and simulation; (b) SF of the measurement and simulation; Green shade marks the component region, pink the setup region.*

The goal of the calibration is to reach a good fit between the structure functions of the measurement and the simulation model, therefore subsequent material tuning was done for each component of the inner structure (Table 2). Since density and heat capacity were shown to be interchangeable, for the sake of simplicity, only the density was varied in the calibration process. A good match was obtained between the two responses (Figure 7).

Table 2. Calibrated material properties

Component (Material)	Density (Kg/m³)	Thermal conductivity (W/mC)	Specific heat (J/kgC)
Die (Silicon)	1800	65	700
Die attach (Solder)	8400	28	210
Slug/Pins (Copper)	8300	380	280
Mold (Plastic)	2000	0.7	820
Wire bonds (Aluminum)	2689	200	951

4.4.2 Automated calibration using optiSLang

The automation process involves two main steps. First, by approaching the topic through a design of experiments (DoE) methodology, a sensitivity analysis is performed within the Ansys Workbench project using the OptiSlang plug-in. The input parameters (thermal conductivity and density of all component structures) are varied while the resulting Z_{th} of the system is monitored.

Second, based on the results of the DoE, optimization algorithms are used to compare the measured Z_{th} with the simulation and to give a prognosis of the best-fit properties for the defined system. The optimization is done by minimizing the difference between measured and simulated Z_{th} curves. Weighting factors were used to focus the optimization on the thermal behavior of the component rather than the measurement setup. Two optimization algorithms are used. The first optimization is done with an Evolutionary Algorithm (EA) for a broader search of the best-fit parameters. The design point with the best fit is then transferred to a Non-Linear Programming by Quadratic Lagrangian (NLPQL) algorithm, which does a finer search around the values determined by the evolutionary algorithm.

A simple diagram of the procedure is presented below.
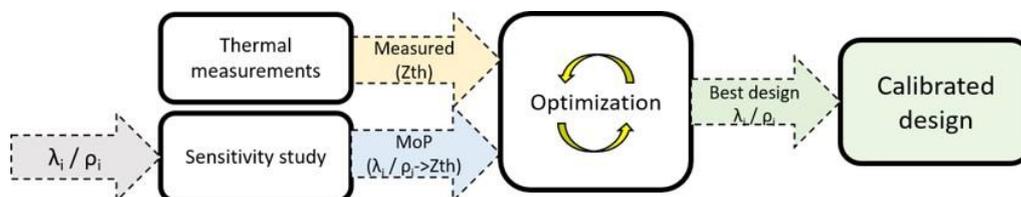
Figure 6. *Optimization diagram*

Comparing the two calibration methods (manual and automated) with the measurement results, a good fit was obtained, both methods leading to similar derived material properties for the component.
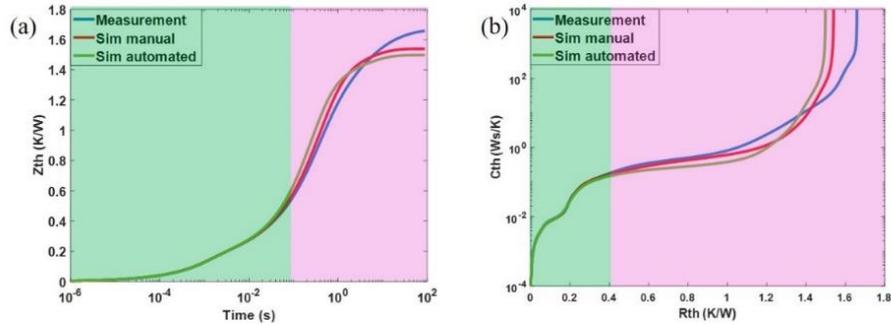
Figure 7. *(a) Zth curves of the measuremnt, manuallly calibrated simulation model and automated calibrated simulation model; (b) SF curves of the measuremnt, manuallly calibrated simulation model and automated calibrated simulation model*

4.5 Conclusions

Two procedures for calibrating FEA models based on thermal measurements of electronic components have been presented and compared. The first calibration method consisted of a manual iterative approach where structure functions were derived from thermal impedance curves based on established methods. Following a comprehensive analysis of the structure functions by varying the material parameters for each structure layer inside the component, a very good agreement was reached between the simulation results and the measurement data. To improve on the performance and repeatability of this method, a second automated calibration method was implemented. In this procedure, an optimization software is coupled to the simulation environment to directly compare the measurement and simulated thermal impedance curves and match them, by varying all the material parameters simultaneously. Not only does this approach led to readily available calibrated models but also it does it in a time-effective and straightforward manner, which reduces the expertise requirements of the user.

Chapter 5

Complete heat path calibration of power MOSFETS via automated optimization
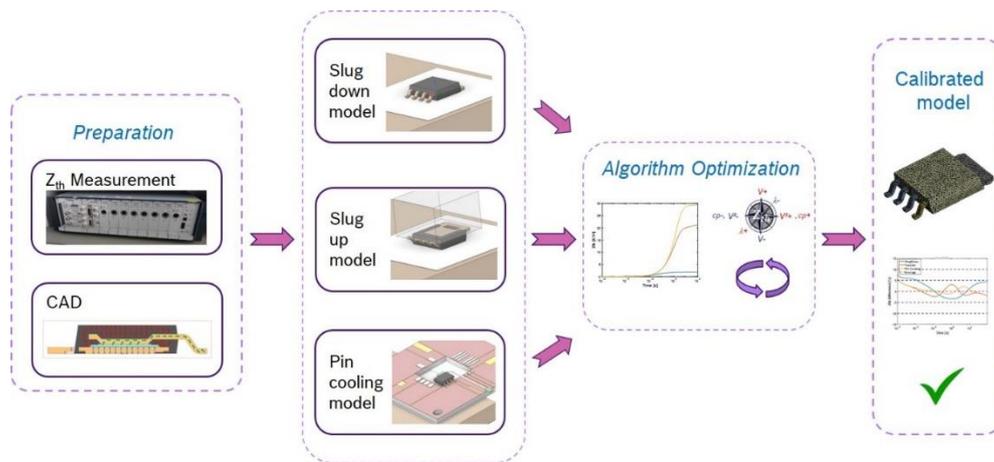
5.1 Introduction

The aim of this chapter is to describe the methodology for the measurement and modeling of power MOSFETS in an automated and standardized way that considers all heat paths through the package. By describing the complete thermal behavior of the packages, it ensures its accuracy in all cooling scenarios it might be used in an ECU model. The measurement setup and methodology described, ensures reliability and repeatability allowing for standardization. Streamlining of the model calibration process is done using optimization algorithms and direct thermal impedance curve fitting. As a result, processing times are lowered and understanding of complex structure function transformations is bypassed.

5.2 Theoretical background

While in the past, a manual iterative approach involving structure function transformations for FEM model calibration has been used, we have also highlighted in the previous chapter a methodology that uses the OptiSlang optimization algorithms for an automated calibration process.

Using these concepts, Z_{th} curves describing the thermal behaviors of power MOSFET packages are measured and adjusted to generate high accuracy FEM models for system level simulations. A schematic representation of the used workflow is presented below in Figure 1.
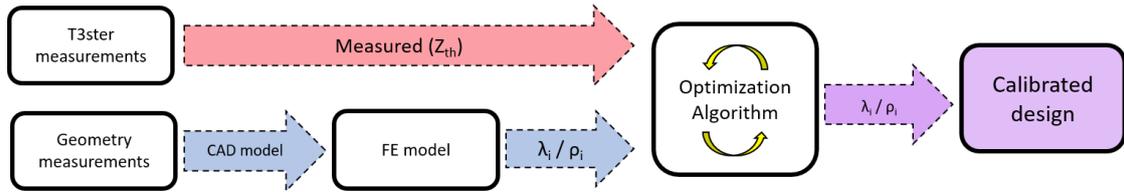
Figure 1. *Calibration workflow schematic*

5.3 FEM modelling

5.3.1 Package description and modelling

The two packages used in exemplifying the methodology outlined in this paper, are an LFPak56 (Figure 2a) and LFPak56D (Figure 2b). Between the LFPak56 and LFPak56D the major difference comes from the presence of two silicon chips in the LFPak56D that leads to a splitting of both the clip and the slug into two parts.

The resulting geometrical models of the two packages built based on the same methodology presented before, can be seen below in Figure 2.
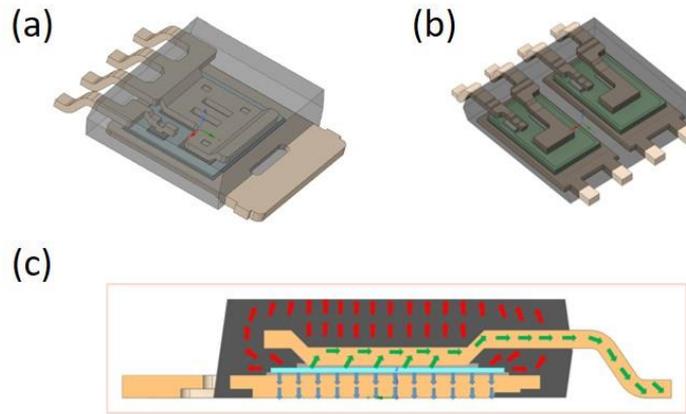
Figure 2. *Geometrical models of (a) BUK7Y1R7-40H LFPak56; (b) BUK7K6R8-40E LFPak56D; (c) Heat paths through package*

Since the calibration methodology in this paper refers to all three-heat paths, separate materials must be defined for both the slug and clip as well as for the bottom and top solder bonds to ensure enough degrees of freedom for the optimizer. For the purpose of calibrating the current models, standard literature properties were used as the starting values for the adjustment properties. Table 1 details these values.

Table1. Initial component material properties

Material properties	Density [kg/m^3]	Thermal cond. [W/(m*K)]	Specific heat [J/(kg*K)]
Silicon	2330	117	700
Solder (chip to slug)	8500	50	176
Solder (chip to clip)	8500	50	176
Copper (slug)	8960	401	385
Copper (clip)	8960	401	385
Mold	1120	0.88	1400

5.3.2 Measurement setup modelling

In order to isolate each heat path and measure its corresponding thermal impedance, three distinct setups were built.

As the methodology in this paper targets the model adjustment of all three heat paths simultaneously, all three set ups are present in the same simulation model (Figure 3). One common set of material properties is used for all three components simulated in the different setups. In this way, any change of a property will influence the response of all three systems.
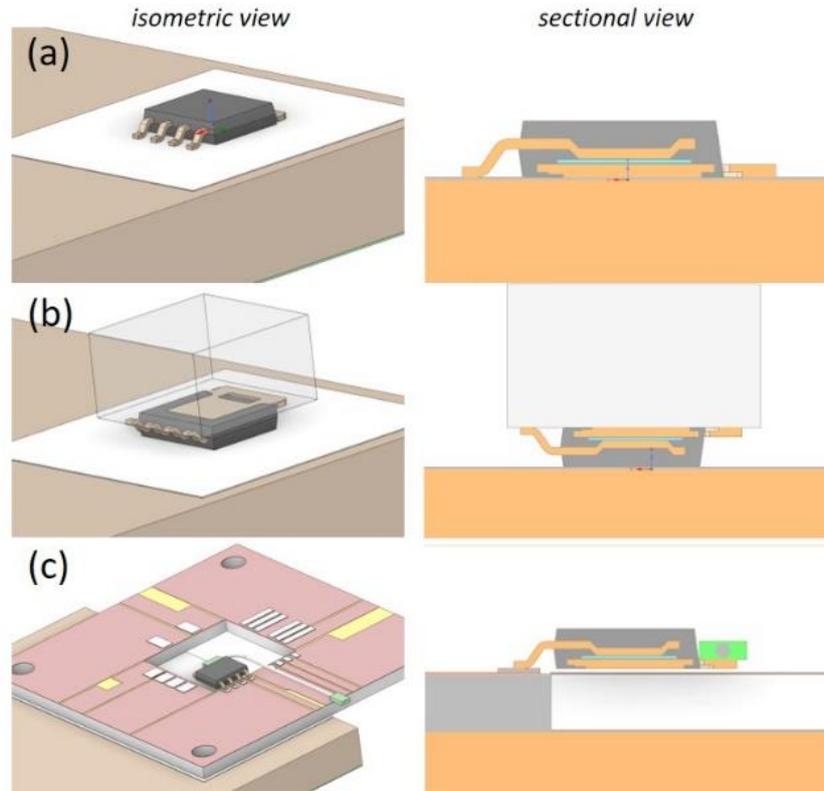
Figure 3. *(a) Model set-up for slug down cooling configuration; (b) Model set-up for topside cooling configuration; (c) Model set-up for through pin cooling configuration;*

5.3.3 OptiSlang methodology workflow

For the model calibration process, the automated process uses OptiSlang as the optimization software similar to the previous chapter.

5.4 Results and discussions

5.4.1 Measurements

A number of five DUTs were used for reference measurements using each setup, totaling a number of 15 measurements. Based on each data set, an averaged Z_{th} curve was calculated for the three configurations (Figure 4).
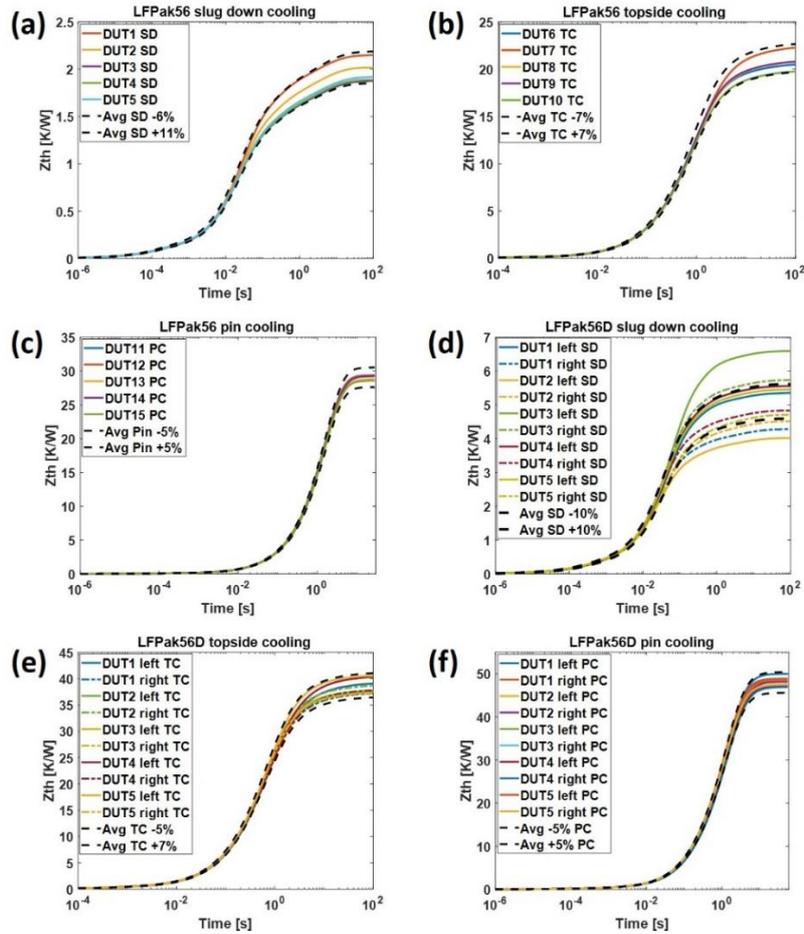
Figure 4. *(a)LFPak56 slug down measurement; (b)LFPak56 topside cooling measurement; (c)LFPak56 pin cooling measurements; (d)LFPak56D slug down measurement; (e)LFPak56D topside cooling measurements; (f)LFPak56D pin cooling measurements*

5.4.2 Automated optimization

For the automated calibration to be successful it is important to have a good representation of the measurement setup, otherwise by trying to force a good fit in the setup contribution to the Z_{th}, the optimizer might compromise accuracy in the component region of the Z_{th}. The model of prognosis (MoP) generated by the sensitivity study, required 67 design points to reach a good coefficient of Prognosis (CoP > 98%). The model was run on a workstation with 20 cores and 512 GB of RAM and required approximately 16 hours to reach the MoP. Compared to the difficult and time-consuming process of manually calibrating each path, the optimization methodology reached a good fit (<10%) in a short time frame.

Table 2 Resulting material property change after calibration

Material properties	Density [kg/m^3]		Thermal cond. [W/(m*K)]	
DUT	LFPak56	LFPak56D	LFPak56	LFPak56D
Silicon	- 66.9%	- 4.0%	- 65.5%	- 39.2%
Solder (chip to slug)	- 27.2%	- 2.5%	- 23.2%	- 21.2%
Solder (chip to clip)	- 30.9%	- 16.5%	- 36.3%	+ 24.0%
Copper (slug)	+ 4.2%	- 25.0%	- 0.2%	- 11.5%
Copper (clip)	+ 7.3%	- 17.6%	- 7.1%	+ 4.7%
Mold	+ 51.6%	+ 34.5%	+ 36.2%	+ 30.7%

The limitation is given by the volume application of the load as this will introduce an initial heat capacity which cannot be corrected. For the LFPak56 we found a good agreement between the slug down configuration resulting from the calibrated properties and the average value of the measurement ranging in a 10% difference for the 0.001 – 0.01s time frame and dropping below 5% for the rest of the time interval. In the topside and pin cooling we found a difference smaller than 5% for the entire time interval. (Figure 5a). Similar results were reached for the second package (LFPak56D) with a difference below 5% from average for all cooling configurations (Figure 5b). This comparison helps us define the accuracy of the models and understand the case usability in complex system simulations.
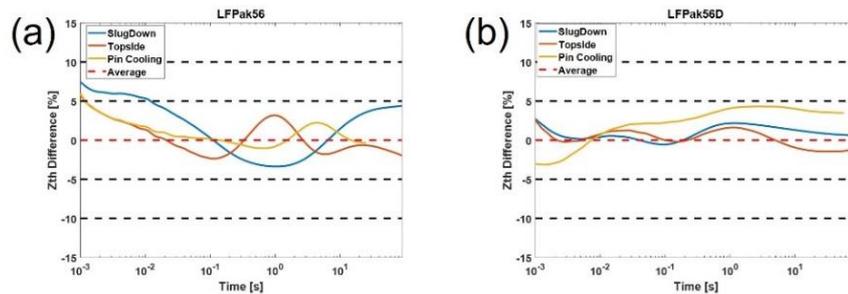
Figure 5. *Zth difference from average measurement for (a)LFPak56; (b)LFPak56D; Zth difference between the model with calibrated properties and with literature properties for (c) LFPak56; (d) LFPak56D.*

Using optimization algorithms brings a significant benefit over the subsequent manual calibration of each heat path. A classical manual approach would require each layer in the heat path to be adjusted in order of their presence in the transfer for each cooling configuration. Using a software based automated calibration allows for generation of a Model of Prognosis based on a pre-defined Design of Experiments which varies all properties for each layer at the same time this can be achieved significantly faster.

5.5 Conclusions

Compared to conventional manual method that requires complex mathematical transformations to understand the heat path and time-consuming repetitive trials to fit material parameters, by using these automated methods the process can be streamlined and standardized. Thus, the process is simplified requiring less input and less deep understanding of the heat path by the user.

By comparing the resulting material properties to generic properties found in literature, significant differences of up to even 60% can occur. This level of errors in approximation, would propagate further into the system simulation rendering the results uncertain. As such, it is highlighted yet again the importance of measuring realistic Z_{th} responses and modelling components with corresponding properties.

In conclusion, while the material properties derived for the models studied in this paper are not universal, as they depend on the exact dimensions used and mesh settings, we have outlined a methodology that can be successfully applied to measuring and modeling any particular MOSFET package.

Chapter 6
Final conclusions

This paper aimed at finding a working concept for building high accuracy component models for the thermal domain to be used further into complex system simulations.

Starting from the first chapter of the paper, the main theoretical concepts related to thermal theory and computer aided design have been introduced and discussed. The fundamental procedure for calibrating any system can be broken down into a few basic steps: i) record a thermal measurement of the device under test, ii) build up a virtual representation of the said device, iii) build up a virtual representation of the said device, iv) set up the initial simulation model, v) adjust the model parameters to fit the measured response.

Chapter two covered a series of crucial points relevant to the fundamental calibration procedure. Through the description of the measured devices, the measurement equipment and setup, the analytical measurements required for CAD generation and a short overview of model setup and calibration approach, the roadmap of the process to be used for specific devices was laid out.

In chapter three, a manual iterative calibration process for the complete heat path (copper slug, copper clip and package mold) was developed using an LFPak88 MOSFET as a test device. The material properties of different layers in the component were adjusted to reach a good match between measured and simulated response in terms of structure functions. The tuned model was checked against an independent measurement for validation, using a PCB test board showing reasonable match with measured data.

The fourth chapter focuses in further developing the methodology to reach an automated procedure. Using a D2Pak as a test vehicle, two procedures for calibrating FEA models based on thermal impedance measurements have been presented and compared. To improve on the performance and repeatability of the iterative method, a second automated calibration method was implemented and tested on the main heat path of the device. In this procedure, an optimization software is coupled to the simulation environment to directly compare the measurement and simulated thermal impedance curves and match them. Not only does this approach led to readily available calibrated models but also it does it in a time-effective and straightforward manner, which reduces the expertise requirements of the user.

The final chapter completes the automated workflow by taking into consideration all three heat paths through a component. Based on two more use cases: an LFPak56 and an LFPak56D, the method was proven successful in reaching the desired accuracy level in a simplified and streamlined manner.

In conclusion, in this paper we have proposed a general methodology for both measuring and calibrating component simulation models for further use in complex systems and

assemblies. We have shown the applicability on different types of packages and what are the challenges encountered for both the measuring and modelling concepts.

While the relevance for each heat path is dependent on application and cooling solutions of the system, a detailed description of the model brings a great benefit in ensuring accurate results for any given configuration. This opens multiple possibilities when it comes to optimizing the thermal design, in terms of thermal performance and manufacturability. The work described in this paper paves the way for standardized methodology in reliable and effective electro-thermal design for the automotive industry and any other electronics development.

References

[1] Ingraham, Joseph C. (24 March 1957). "Automobiles: Races; Everybody Manages to Win Something At the Daytona Beach Contests". The New York Times. p. 153. Retrieved 1 May 2015.
[2] "The Rambler Rebel's fuel injection – The Dream and the Legend". Hemmings. 27 June 2017. Retrieved 8 November 2018.
[3] Benrey, Ronald M. (October 1971). "Microelectronics in the '70s". Popular Science. Bonnier Corporation. 199 (4): 83–5, 150–2. ISSN 0161-7370.
[4] https://www.statista.com/statistics/277931/automotive-electronics-cost-as-a-share-of-total-car-cost-worldwide/#statisticContainer
[5] https://www.bosch.de/unser-unternehmen/bosch-in-deutschland/salzgitter/
[6] Electronic Failure Analysis handbook, Perry L. Martin chapters 1.1 – 1.5
[7] Lienhard, J.H., Lienhard, J.H., 2011. A heat transfer textbook, 4th ed. ed. Dover Publications, Mineola, N.Y
[8] "Transient dual interface test method or the measurement of the thermal resistance junction to case of semiconductor devices with heat flow through a single path", JEDEC Standard JESD51-14, Nov. 2010.
[9] V. Székely "A new evaluation method of thermal transient measurement results", Microelectronics Journal issue 3, vol. 28, p.277-292
[10] Sümegi Ambrus, "Calibration of temperature sensitive parameter at high currents", BSc Thesis
[11] Zienkiewicz, O.C., Taylor, R.L., Zhu, J.Z., 2013. The finite element method: its basis and fundamentals, Seventh edition. ed. Elsevier, Butterworth-Heinemann, Amsterdam.
[12] https://www.nexperia.com/products/mosfets/automotive-mosfets/
[13] https://www.infineon.com/cms/en/product/packages/PG-TO263/PG-TO263-7-3/
[14] Mohan, N., Undeland, T.M., Robbins, W.P., 2003. Power electronics: converters, applications, and design, 3rd ed. ed. John Wiley & Sons, Hoboken, NJ, 571-581;
[15] Most, T. and J. Will (2008). Metamodel of Optimal Prognosis - an automatic approach for variable reduction and optimal metamodel selection. In Proc. Weimarer Optimierungs- und Stochastiktage 5.0, Weimar, Germany, November 20-21, 2008.
[16] Schittkowski, K. (1986). NLPQL: A Fortran subroutine for solving constrained nonlinear programming problems. Annals of Operations Research 5, 485–500.
[17] Sz. Szőke, Z. Kórádi, "Component Model Calibration Using Transient Thermal Test Methods and Multiple Measurement Setups", 25th International Workshop Thermal Investigations of ICs and System (Therminic 2019)

Appendix – List of publications

Journal Publications

R. Cioban, Sz. Szőke, D. Zaharie-B, Z. Kórádi, C. Leordean, S. Simon, "FEM model calibration for simulation aided thermal design," Microelectronics Reliability, Volume 118, 2021, 114042, ISSN 0026-2714, https://doi.org/10.1016/j.microrel.2021.114042, (**IF 1.589, AIS 0.293**)

R. Cioban, Sz. Szőke, D. Zaharie-B, Z. Kórádi, C. Leordean, S. Simon, "Finite element thermal modelling of power MOSFET packages," Microelectronics Reliability, submitted with manuscript number: MICREL-D-22-00024R2, 2022 (**IF 1.589, AIS 0.293**)

Conference Publication

R. Cioban, S. Szöke, Z. Kórádi, D. Zaharie-B. and C. Leordean, "Validated Model Calibration for Simulation Aided Thermal Design," 2020 36th Semiconductor Thermal Measurement, Modeling & Management Symposium (SEMI-THERM), 2020, pp. 114-123, doi: 10.23919/SEMI-THERM50369.2020.9142853.